AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the Application.

LISTING OF CLAIMS:

1. (Currently amended) A memory array with byte-alterable capability comprising:

a plurality of adjacent cells each comprising,

a select gate metal oxide semiconductor field effect transistor, MOSFET device, and

a split-gate memory cell whose source is connected to the drain of said select gate MOSFET device wherein the gate of said select gate MOSFET device is controlled independently of the gate of said split-gate memory cell,

select lines connecting the select gate of the select gate MOSFET device of one of the plurality of adjacent cells to the select gate of the select gate MOSFET device of an adjacent one of the plurality of adjacent cells.

2. (Original) The memory array with byte-alterable capability of claim 1 further comprising:

bit lines which are tied to the drains of said split-gate memory cell.

3. (Original) The memory array with byte-alterable capability of claim 1 further comprising:

source lines which are tied to the sources of said select gate MOSFET devices.

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4. (Original) The memory array with byte-alterable capability of claim 1 further comprising:

word lines which are tied to control gates of said split-gate memory cell.

5. (Cancelled).

6. (Original) The memory array with byte-alterable capability of claim 1 wherein said control gate MOSFET contains a floating gate which is insulated from said control gate by a dielectric insulating material such as silicon dioxide.

7. (Original) The memory array with byte-alterable capability of claim 6 wherein said split-gate memory cell contains a source region which is also the drain for said select gate MOSFET device.

8. (Original) The memory array with byte-alterable capability of claim 6 wherein said control gate MOSFET contains a drain region.

9. (Original) The memory array with byte-alterable capability of claim 6 wherein said control gate MOSFET contains a control gate which is insulated from said floating gate by a dielectric insulating material such as silicon dioxide.

10. (Original) The memory array with byte-alterable capability of claim 6 wherein said control gate contained in the control gate MOSFET device is insulated from said drain of said control gate MOSFET device by a dielectric insulating material.

11. (Original) The memory array with byte-alterable capability of claim 1 wherein said select gate MOSFET contains a select gate which is insulated from said select gate drain region and said selected gate source region by a dielectric insulating material.

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12. (Currently Amended) The memory array with byte-alterable capability of claim 1 wherein [[said]] the bits of [[said]] the bytes have a common source line.

13. (Currently Amended) The memory array with byte-alterable capability of claim [[1]] 12 wherein said source [[lines]] line common to said bytes have a high voltage applied to inhibit erase of said cells of [[said]] unselected bytes.

14. (Currently Amended) The memory array with byte-alterable capability of claim [[1]] 13 wherein said source lines common to said bytes have a low voltage applied to enable an erase of said cells of said un selected bytes.

15. (Currently Amended) The memory array with byte-alterable capability of claim [[1]] 14 wherein the erasure of selected bytes requires a high voltage on said selected gates associated with the selected bytes.

16. (Currently Amended) The memory array with byte-alterable capability of claim [[1]] 15 wherein the erasure of selected bytes requires a high voltage on said control gates.

17. (Currently Amended) The memory array with byte-alterable capability of claim [[1]] 12 wherein the programming of selected cells of said selected bytes require high voltage on said select gate, a lower voltage on said control gate and a high voltage on said source line.

18. (Original) The memory array with byte-alterable capability of claim 17 wherein said word lines common to said bytes have a zero voltage applied to inhibit programming of unselected cells.

Claims 19-43 (withdrawn).

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